Looking back at the IWLS 1997 Focus Groups

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1. Introduction

At the 1997 IWLS the first of a continuing series of focus groups was held. This was a unique opportunity to ask the world leaders in the logic synthesis field about their views on the state of the art in this discipline. All participants were divided in 10 groups, and each group was giving the following five questions:

1. What are the five most important theoretic contributions to Logic synthesis. ? (and why)
2. What are the five most important practical contributions to Logic synthesis. ? (and why)
3. What are the three most useless subjects addressed in the last decade of logic synthesis research ? (and why)
4. What are the three most important issues presented/discussed at this symposium ? (and why)
5. What will be the three most important subjects going to be discussed at IWLS-2002 ?

The results from all groups were combined to compile an aggregate view of the community. In this paper we will review the summary of these results. The figures in the following paragraphs show the major items and the number of groups that listed them in their top 5. In section 5, we will comment on what predictions came through, and which ones did not. Finally, the appendix of this paper archives the detailed result from all groups, to ensure that this information gets preserved for the logic synthesis community.

2. Theoretical Contributions

Two-level minimization was most widely recognized as the most important theoretical contributions to logic synthesis. The introduction of BDDs, algebraic optimization and the use of

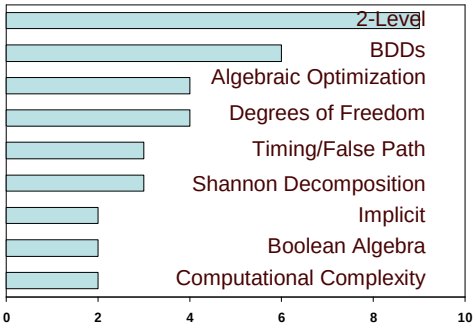

Figure 1 Theoretical Contributions

various degrees of freedom (e.g. don't cares) contribute significantly to the body of knowledge that underlies modern logic synthesis systems. Three groups mentioned the importance of timing and false path analysis.

3. Practical Contributions

BDDs, besides being a major theoretical contribution, made the top of the list of practical contributions. Techniques like dynamic variable ordering have made them particularly useful in a synthesis context. Widely available systems like Espresso and MIS allowed many students to have a first hand experience with a practical synthesis system. Technology mapping, really filled a void: how to bridge from a technology independent netlist to a technology implementation. The first practical use of logic synthesis was mostly in technology mapping. The introduction of RTL synthesis greatly increased the need for more powerful logic optimization. Much less optimal networks appeared at the input to the logic synthesizers, due to wide use of inefficient RTL language structures. Retiming is the only sequential synthesis algorithm that has been of practical use, especially in FPGAs and in designs described at behavioral levels.

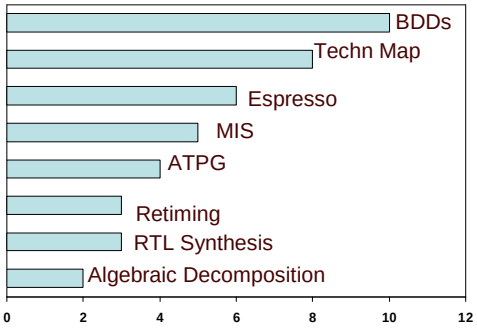

Figure 2 Practical Contributions

4. Overvalued Concepts

Quite a few groups felt compelled to rephrase the question on useless subjects into: what are the most controversial issues, or what are some of the more overvalued concepts in synthesis research. The explosion of BDD variants was certainly on all groups their lists. While the flood of papers from the mid nineties has stopped, new variants still pop up. Most of the synthesis work on Low Power was not deemed very useful. However, things might be changing here. Nowadays, the process technologists are providing us with interesting options such as multi-voltage libraries, multi-threshold libraries, voltage and power-islands, and micro-architects are much more conscious in adding clock-gating information. Both of these provide significant optimization opportunities for synthesis tools. Especially when traded off against performance and signal integrity (noise) constraints.

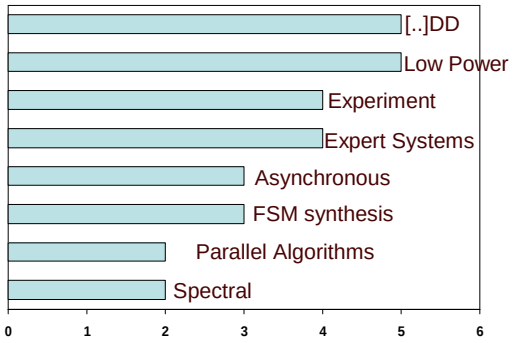

Figure 3 Overvalued Contributions

Experiments, e.g. benchmarks remain a major problem. Nearly all IWLS-02 papers still cite the old, small, beaten-to-death benchmarks results. Despite various efforts in reviving the benchmarks and adding a benchmark chair to the IWLS, we still have not made much progress here. Expert systems have not really worked for logic synthesis problems. Finite State machine synthesis has not moved beyond the state it was in 1997. Parallelizing synthesis has not taken off, but we should seriously look at the possibilities that new GRID infrastructures will provide us in an on-demand computing world.

5. Predictions for IWLS-2002

How well did we do in predicting the topics for IWLS02? Figure 4 shows the top 5 predicted areas, in 1997. Let us compare these to the content of the actual workshop in 2002 [1]. The IWLS02 opening session was on Structured Logic Synthesis, directly in line with the DSM theme as predicted. Session 2 was on reconfigurable architectures. Verification and synthesis continue to share significant portions of the underlying algorithms and datastructures, a theme that is indeed present in many papers and posters at IWLS02. Synthesis and design for better verifiability has not really taken off. But maybe we were too early in our predictions. The verification community is pushing hard for assertion based specifications. Several languages are being supplemented with assertions and new languages to specify properties have been standardized. It starts to be time that we take advantage of this in synthesis as well.

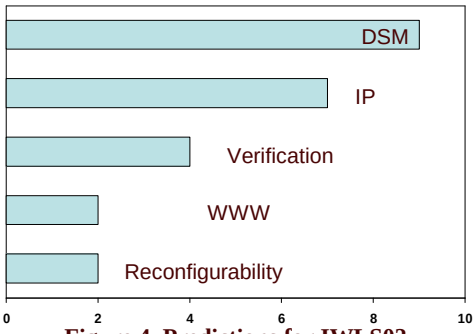

Figure 4 Predictions for IWLS02

The Web-theme has not had a real impact, except for the presentation on Web based BDD visualization. The whole IP reuse theme seems to have largely bypassed the logic synthesis community, and has had little impact on synthesis research.

6. Acknowledgments

My thanks to all participants of the 1997 IWLS focus groups.

7. References

[1] Proceedings of the 11th IEEE/ACM International workshop on Logic synthesis, June4-7, 2002. New Orleans.

8. Appendix: Detailed Group Results

8.1.1 GROUP 1

Q1: Main Theoretical Contributions:

1. Quine - McClusky Method
2. Shannon/Boole Decomposition
3. Exact Timing Analysis
4. State Minimization of Incompletely specified state machines
5. Don't Cares

Q2: Main Practical Contribution:

1. Decision Diagram Data structure
2. Retiming
3. Heuristic Multi-level Minimization
4. Tree Mapping
5. RTL --> Logic

Q3: Controversial Issues

1. [A-Z]*[d-W]*[.3-T-2T]*DDs
2. Spectral Transformation/RM transformation
3. Overselling of Power
4. Overselling of Synth. of Asynchronous
5. Use of PROLOG for Logic Synthesis/Verification

Q4: Contributions From This Workshop.

1. Advances in solution for SAT/covering problems
2. DSM/Combinational/Sequential/Logic/Physical Synthesis

Q5: Destination 2002!

1. VUDSM
2. Layout Driven Synthesis
3. Chip Level Verification
4. New Circuit Families
5. Noise Issues
6. Synthesis for Manufacturability, Reliability
7. Hardware Reuse
8. Java (TM) based distributed design flow.
9. Quantum Computing
10. DNA computing (look at us)

8.1.2 GROUP 2

Q1: Five Most Important Theoretical Contributions

1. Theory of Algebraic Optimization
2. Implicit Set Manipulation
3. Theory of Flexibility in Logic Optimization
4. Multifault Testability
5. False Path Analysis

Q2: Five Most Important Practical Contributions

1. Major Milestones in Logic Synthesis Tools: - LSS => MIS/SIS => Synopsys Design Compiler
2. BDD Methods

3. Practical Research Environment: - Availability of University S/W / Standard Languages/Benchmarks/IWLS
4. Espresso and Heuristic Minimization
5. SAT Solvers

Q3: Three Most Useless Subjects

1. Reargued, Unscalable Research Directed Specifically at Bogus Benchmarks - Optimization of 10 State FSMs - (Bad) Research in Low Power at the Gate Level
2. VERILOG/UHDL Split

Q4: Three Most Important subjects at IWLS 97

1. DSM
2. Timing Analysis
3. Satisfiabiity and Covering

Q5: Three Most Important Subjects at IWLS 02

1. IP/System on a Chip
2. VDSM
3. Synthesis Methodology for Verifiability

8.1.3 GROUP 3

Q1 The 5 Most Important Theoretical Contributions

1. Two Level Logic Minimization: Quine- McCluskey, Boole/ Shannon, UCP, (Espresso?)
2. Mathematical Models of Logic Circuits: Boolean Algebras, Boolean Networks, Mealy- Moore FSMs,Multi- Valued Logic, Kernels/ Co- Kernels, etc
3. Synthesis degrees of freedom: SDC/ ODC, Permissible Functions, Boolean Relations, (SPFDs)
4. Critical Path Analysis: Static/ Dynamic Timing Analysis, False Path Analysis
5. Retiming: Leiserson- Rose- Saxe, et seq

Hey! What about BDDs??

Q2 The 5 Most Important Practical Contributions

1. Peephole Optimization: Local Transformations, Rules-Based
2. Algebraic Decomposition:Fast (and good) restructuring, encoding, synthesis for testability
3. BDDs: Combinational and Sequential Verification, symbolic simulation, generalized cofactors, ...
4. Technology Mapping: Tree and DAG Covering, Dynamic Programming (Lehman-Watanabe)
5. Acceleration of ATPG and Combinational Verification: Learning/ Implications, Equivalence Points, Cuts/ heaps/ sweeps

Hey! What about Symbolic FSM Traversal???

Q3 The 3 Most Useless Areas

1. FSM- Synthesis: The Minimize- Encode- Synthesize paradigm is a hoax for multi- level networks-- it doesn't work
2. Asynchronous Synthesis is Pointless
3. Misguided Attempts: Bad Models (Spectral Methods, Neural Nets, Roth- Karp)
4. Generic Optimizers (Expert Systems, Sim. Annealing, Genetic)

Hey! What about Benchmark Abuse???

Q4 The 3 Most Important Issues at IWLS97

1. Covering Problems: Negative Thinking
2. Deep SubMicron
3. Panel Discussion
4. Linear Placement paper is a start
5. Configurable Hardware Solutions satisfiability, implications, etc

Hey! TBDDs and re-encoding of the input domain???

Q5 The 3 Most Important Issues at IWLS02

1. Error Diagnosis: Design Convergence, Engineering Changes (ECOs), Incremental Design, rewire without replacement
2. Synthesis of Communicating Subsystems, Emphasis shifts to wiring, IP blocks come as- is
3. On- the- Fly Re- Programmability

Hey! What about verification- ECOs,and the Pentium Bug???

8.1.4 Group 4

Q1: 5 Most Important Theoretic Contributions

1. Expresso/Quine - McCluskey
2. BDDs (Bryant)
3. Application of Computation Complexity
4. See contribution #5.
5. See contribution #6.

Q2: 5 Most Important Practical Contributions

1. BDD Algorithms
2. Implication Methods and Other ATPG Algorithms (Recursive Learning, Redundancy Addition/Removal)
3. 2-Level Optimization (Expresso)
4. Public Domain Software (*IS, BDD Packages)
5. Technology Mapping and Post-Mapping Optimization (Socrates, LUT-Based Packages)

Q3: 3 Most Useless Issues in the Last 10 Years

1. Experimental Noise Dominating the Accuracy of the Mode (Delay Models, Power Analysis, Retiming)
2. Misleading and Misinterpreted Experimental Results => Need for CAD Community to be More Accepting of Negative Results (Within Reason)
3. Overuse and Overgeneralization of BDDs (E.g., Canonicity of BDDs Not Required for the Problem, "Alphabet Soup of BDDs" - Randal Bryant)

Q4: 3 Most Important Issues at IWLS/97

1. BDDs and Applications
2. Pass Transistors
3. Functional Verification

Q5: 3 Most Important Subjects at IWLS - 2002

1. Design Convergence (Physical Design and Logic Synthesis)
2. Interface Analysis and Modeling for IP Design
3. Managing/Abstracting Large Designs
4. Web-Based Design
5. Focus Group Speaker Designation Avoidance

8.1.5 Group 5

Q1: Theoretical Contributions

Given Seminal Work on Models

1. Quine - McCluskey
2. Algebraic Decomposition - (Exponential Reductions)
3. Transduction Method - (Link Structure and Function)
4. Symbolic Minim and Constrained Enc. - (Need FSMs)
5. BDDs - (Efficient Canonical Repr.)

Q2: Practical Contributions Given

1. Lots of Useful/less Theory
2. Espesso
3. Tree-Based Techmap
4. MIS IN Public Domain - (Otherwise No synopsys)
5. Efficient Impl. of BDDs/Sifting - (Otherwise Can't Beat Synopsys)
6. Retiming - Neat, Polynomial...

Q3: Useless Subjects

1. Asynchronous Circuits Would Win Now But Nobody Ready To Bet On It
2. Lower Power Logic Synthesis - (Minimal Improvement, Questionable Model/Cost Function)
3. False Paths - (Nobody uses It, Although It's Neat...)
4. Genetic Algorithms - (Orgies and Immoral...)

Q4: Most Important Issues Now

1. Interaction B/W Synthesis ad Physical Design - (Can't Decouple)
2. System-Level Interface Design - (Should Decouple...)
3. Feedback From Designers - (Did You See Any?)

Q5: 5 Years From Now

1. Interaction between Synthesis & Physical Design - (Controversial...)
2. Communication Synthesis - (IP Integration - What A Lovely Keyword)
3. Reconfigurable Logic - (Need Something Well...) Loo, Ma... No BDDs!

8.1.6 Group 6

Q1: Most Important Theoretic Contributions

1. Two-level Logic Minimization
2. Multi-level Logic Optimization, Algebraic Transform
3. BDD's, Representations of Logic functions
4. Timing Analysis, False Paths
5. Don't Cares, Boolean Optimization Techniques

Q2: Most Important Practical Contributions

1. FPGA's, Concept, Tools
2. Tools for 2-level Minimization (express)
3. Tools for Multi-level synthesis (MIS, SIS)
4. Delay Models, Performance Optimization Techniques
5. BDD Packages

Q3: Most Useless Subjects

1. Theory for Power Estimation/Reduction in Logic Synthesis
2. Exotic BDD's (Too Many!)
3. ISCAS Benchmarks (*)

Q4: Most Important Issues Presented at IWLS '97

1. Efficient Solutions to Basic Problems - (SAT, Covering, Coloring, ILP)
2. Layout-oriented Synthesis, Integration
3. Alternative Design Styles - PTL, Domino

Q5: Topics for IWLS' 2002

1. Drastically New Design Methodology
2. Linking Logic with layout, Integration
3. Moving Toward Full Custom, Transition Level Design Styles

8.1.7 Group 7

Q1: Theoretical Contributions

1. Sequential Optimization (State Assignment, DeMicheli, Retiming, Leiserson/Saxe)
2. Two-level and Multi-level Logic Minimization - Quine-McCluskey, ODC-based node simplification, ATPG-based Techniques)
3. Kernel Extraction - (Brayton and McMullen)
4. Verification - (Combinational, Automated-based)
5. Binary Decision Diagrams and Some of Its Variants - (Acker, Bryant, etc.)

Q2: Practical Contributions

1. Technology Mapping
2. Espresso/MIS
3. BDD-based Algor
4. Redundancy Removal Techniques
5. Retiming

Q3: Overvalued Concepts/Algorithms

1. Too Many Variants on BDD's
2. Parallel Cad Algorithms
3. Expert Systems for CAD

Q4: Best IWLS Papers

1. Paper 3 in Session 3 (DDs and PTL)
2. ?

Q5: Future Areas of Interest

1. Links Between Physical Design and Logic Synthesis
2. Hierarchical/Incremental Synthesis
3. Mixed-domain Systems (Analog, Digital, Mechanical, etc.)

8.1.8 Group 8

Q1: Five Most Important Theoretical Contributions

1. Boolean Algebra
2. Two-level Logic Optimization
3. Algebraic Methods of Multi-level - Logic Synthesis
4. Complexity Theory
5. BDD - Automata Theory

Q2: Five Most Important Practical Contributions

1. Interactive Synthesis Tool
2. BD Package
3. Technology Mapping
4. ATPG
5. "Library-based" Design - ASICs, Programmable Devices

Q3: Three Most Useless Subjects

1. UDL/1
2. Hardware Accelerator
3. Parallel Algorithms

Q4: Three Most Important Issues at IWLS '97

1. The "Interaction" between Logic Synthesis and Physical Design
2. Verification
3. Functional Decomposition

Q5: Three Most Important Subjects in 2002

1. Intellectual Property
2. Application of Logic Synthesis to Other Areas and New Devices
3. New Application of Data Structure

8.1.9 Group 9

Q1: Theoretical Contributions

1. Boolean Calculus
2. Switching Theory (Shannon)
3. Quine-McClusky EII Minimization
4. Automata Theory
5. Implicit Techniques in Set/Relation Manipulations

Q2: Practical Contributions

1. Algebraic Decomposition Applied to Technology Independent Multi-level Logic Synthesis
2. Technology Mapping
3. BDDs (ROBDDs)
4. Hardware Description Languages
5. 2-Level Logic Minimization

Q3: Useless Stuff.

1. Logic Synthesis for Low Power - 5% Power Deduction in 10% Power Component - XW -> 0.995 XW
2. State Encoding/Minimization - Who Uses It?
3. Alphabet Soup of BDDs - ???? BDD (26x26x26x26 > 100,000)

Q4: Important Issues At This Symposium

1. Logic Synthesis for High Performance
2. Link Between Logic Synthesis and Physical Design
3. Search Techniques

Q5: Issues for IWLS 2005

1. Modeling Physical Effects at the Logic Level - (Wiring Cost, Noise, Wiring Delay)
2. Support for Design Reuse/Design Change
3. Support for Efficient Design Validation at Higher Levels of Abstraction

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8.1.10 Group 10

Q1: Theory

1. Karnaugh Maps. Q-M
2. Unate Recursive Paradigm
3. Dynamic Prog. Tree Cover
4. Data Structures for Boolean Functions
5. FSM and Language Based Design

Q2: Practice

1. Espresso
2. Dagon/MIS
3. *BDD packages
4. RTL Synthesis

Q3: Now Important

1. FPGA Based SAT
2. Change Tools
3. Synthesis and Physical Design Papers?
4. Synthesis of Non-Static CMDS

Q4: Useless

1. Graphical FSM Design - Not Useful Enough to
2. Synthesis for Low Power Not the Way to Get Real Savings
3. Design for Test/Synthesis for Test, Is This the Right Problem Tomorrow? Today?

Q5: Looking Forward - 2002

Hierarchal Design

1. Blocks
2. Functions
3. Subroutines

Implementations Repartition

1. Re-encode signal/bus - Physical Issues - H/S Co-Synthesis
2. Timing disciplines (Sync + Async + ...)
3. Verification Functional and Timing