The 14th International Workshop on Logic & Synthesis (IWLS)

June 8 – 10, 2005

Lake Arrowhead, California

Colocated with DAC 2005 (the week before)

www.iwls.org

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The International Workshop on Logic and Synthesis provides an international forum for promoting research and exchanging ideas about all aspects of integrated circuit and system synthesis, optimization, and verification. The workshop encourages early dissemination of ideas and results. Accepted papers are distributed only to IWLS participants.

Topics of interest include architectures and compilation, synthesis and optimization, power and timing analysis, design validation and verification, and design experiences, all applied at system description levels ranging from transistors to hardware-software interfaces. Implementation might be in synchronous or asynchronous CMOS, or any emerging technology. Submissions on modeling, analysis and tools targeting emerging technologies and platforms are particularly encouraged.

Authors may submit complete papers for their proposed presentation. These must be no longer than 8 pages, double column, and in a 10-point font. We also encourage submissions of extended abstracts in the early stages of research that highlight important new problems, perhaps without providing complete solutions. Only electronic submissions will be accepted: submit at http://www.iwls.org. For questions, contact IWLS_pcchair@sigda.org. For travel grants, apply to ACM/SIGDA's travel grant program at http://www.sigda.acm.org/Programs/TravelGrant/.

The workshop format includes paper presentations, posters, invited talks, and social lunch and dinner gatherings. To further stimulate interaction among participants, the upcoming workshop will feature recreational activities replacing the former function of focus groups.

(Extended) Submission deadline for papers and problems	March 14, 2005
Notification of acceptance	April 14, 2005
Final version due	April 28, 2005

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