Call for Participation

The 20th International Workshop on Logic & Synthesis

June 3 – June 5, 2011
University of California, San Diego
La Jolla, CA

www.iwls.org

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The International Workshop on Logic and Synthesis is the premier forum for research in synthesis, optimization, and verification of integrated circuits. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop accepts complete papers as well as abstracts, highlighting important new problems in the early stages of development, without providing complete solutions. The emphasis is on novelty and intellectual rigor.

Topics of interest include: synthesis and optimization; power and timing analysis; testing, validation and verification; architectures and compilation, design experiences and emerging technologies.

Information regarding registration and the workshop venue can be found on the website: `http://www.iwls.org`. Advanced registration is $200 for students and unemployed professionals, $300 for ACM/IEEE members and $400 for non ACM/IEEE members. The registration fee covers all meals and the social event on Saturday evening.

The technical program consists of 21 regular talks, 4 poster presentations, three invited talks and a special session. The invited talks cover emerging topics such as security, post-silicon validation and technological disruption. Note that accepted papers are distributed only to IWLS participants.

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