Cross-Layer Resilient Design for Extreme Scaling and Beyond

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Abstract

As the CMOS feature enters the era of extreme scaling (14nm, 11nm and beyond), the printability challenges are exacerbated. Meanwhile, the vertical scaling with 3D-IC integration using through-silicon-vias (TSVs) has gained tremendous momentum and initial industry adoption, which can further extend the Moore's Law even the horizontal scaling stops ultimately. However, as TSV involves disruptive manufacturing technologies, new modeling and design techniques need to be developed for reliable 3D IC integration. This talk will first show how the nanolithography envelope is being pushed with novel design/process integration for multiple patterning lithography as well as other emerging technologies. In 3D-IC, TSV induced thermal mechanical stress not only results in systematic performance variations, but also leads to mechanical and electrical reliability concerns. Cross-layer full-chip/package modeling and physical design/synthesis techniques will be discussed to achieve reliable 3D-IC integration.

Biography

David Z. Pan received his Ph.D. in computer science from UCLA in 2000. He was a Research Staff Member at IBM T. J. Watson Research Center from 2000 to 2003. Since 2003, he has been with the Department of Electrical and Computer Engineering, UT Austin. He has published over 175 refereed journal and conference papers. He has served as an Associate Editor for IEEE Transactions on CAD, IEEE Transactions on VLSI, IEEE Transactions on CAS - I & II, IEEE CAS Society Newsletter, Science China Information Sciences, Journal of Computer Science and Technology. He has served as Chair of the IEEE CANDE Committee and the ACM/SIGDA Physical Design Technical Committee, Program/General Chair of ISPD, TPC Subcommittee Chair for DAC, ICCAD, ASPDAC, ISLPED, ICCD, ISCAS, and so on. He is a working group member of the *International Technology Roadmap for Semiconductor* (ITRS).

He has received a number of awards, including DAC Top 10 Author in Fifth Decade, DAC Prolific Author Award, 9 Best Paper Awards (ASPDAC 2012, ISPD 2011, IBM Research 2010 Pat Goldberg Memorial Best Paper Award in CS/EE/Math, ASPDAC 2010, DATE 2009, ICICDT 2009, SRC Techcon in 1998, 2007 and 2012), Communications of the ACM Research Highlights (2013), ACM/SIGDA Outstanding New Faculty Award (2005), NSF CAREER Award (2007), SRC Inventor Recognition Award three times, IBM Faculty Award four times, UCLA Engineering Distinguished Young Alumnus Award (2009), ISPD Routing Contest Awards (2007), eASIC Placement Contest Grand Prize (2009), ICCAD'12 CAD Contest Award, among others. He was an IEEE CAS Society Distinguished Lecturer for 2008–2009.