Call for Papers

The 22st International Workshop on Logic & Synthesis

June 7 – June 8, 2013

Austin, TX

www.iwls.org

Sponsored by IEEE and ACM/SIGDA.

The International Workshop on Logic and Synthesis is the premier forum for research in synthesis, optimization, and verification of integrated circuits. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop accepts complete papers highlighting important new problems in the early stages of development, without providing complete solutions. The emphasis is on novelty and intellectual rigor.

Topics of interest include (but are not limited to): synthesis and optimization; power and timing analysis; testing, validation and verification; architectures and compilation; and design experiences. Submissions on modeling, analysis and synthesis for emerging technologies are also encouraged.

Only complete papers with original and previously unpublished material are permitted. Submissions must be no longer than 8 pages, double column, 10-point font. Accepted papers are distributed only to IWLS participants. The workshop format includes paper presentations, posters, invited talks, lunch and dinner gatherings, and recreational activities. Submissions are made electronically through the EDAS system. Please see the website for instructions: `http://www.iwls.org`

You must register the paper by submitting an abstract before the deadline below

Paper abstract submission	March 8, 2013
Full paper submission	**March 15, 2013 - 11.59pm Hawaii Standard Time**
Notification of acceptance	April 1, 2013
Final version due	May 10, 2013

The submission deadline of March 15, 2013 is final, there will be no extension.

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