Call for Papers



The 23rd International Workshop on Logic & Synthesis

May 30 – June 1, 2014

Galleria Park Hotel, San Francisco, CA WWW.iwls.org

The International Workshop on Logic and Synthesis is the premier forum for research in synthesis, optimization, and verification of integrated circuits and systems. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop encourages early dissemination of ideas and results. The workshop accepts complete papers highlighting important new problems in the early stages of development, without providing complete solutions. The emphasis is on novelty

Topics of interest include, but are not limited to: hardware synthesis and optimization; software synthesis; hardware/software co-synthesis; power and timing analysis; testing, validation and verification; synthesis for reconfigurable architectures; hardware compilation for domain-specific languages; design experiences. Submissions on modeling, analysis and synthesis for emerging technologies and platforms are particularly encouraged.

Only complete papers with original and previously unpublished material are permitted. Submissions must be no longer than 8 pages, double column, 10-point font. Accepted papers are distributed only to IWLS participants. The workshop format includes paper presentations, posters, invited talks, social lunch and dinner gatherings, and recreational activities. Submissions are made electronically through EasyChair. Please see the workshop website for instructions: http://www.iwls.org

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You must register the paper by submitting an abstract before the deadline below

Paper abstract submission February 28, 2014

Full paper submission March 7, 2014 - 11.59pm Anywhere on Earth

Technical Program Committee

Notification of acceptance April 4, 2014 Final version April 25, 2014

The submission deadline is final and there will be no extensions.



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