

Call for Papers

The 29th International Workshop on Logic & Synthesis (IWLS)

July 18 – 19, 2020

Moscone Center, San Francisco, CA

www.iwls.org

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The International Workshop on Logic and Synthesis is the premier forum for research in synthesis, optimization, and verification of integrated circuits and systems. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop encourages early dissemination of ideas and results. The workshop accepts complete papers highlighting important new problems in the early stages of development, without providing complete solutions. The emphasis is on novelty and intellectual rigor.

Topics of interest include, but are not limited to: hardware synthesis and optimization; software synthesis; hardware/software co-synthesis; power and timing analysis; testing, validation and verification; synthesis for reconfigurable architectures; hardware compilation for domain-specific languages; and design experiences. Submissions on modeling, analysis and synthesis for emerging technologies and platforms are particularly encouraged.

Only complete papers with original and previously unpublished material are permitted. Submissions must be no longer than 8 pages, double column, 10-point font. Accepted papers are distributed only to IWLS participants. The workshop format includes paper presentations, posters, invited talks, social lunch and dinner gatherings, and recreational activities. Submissions are made electronically through EasyChair. Please see the workshop website for instructions: <http://www.iwls.org>.

Paper abstract submission	April 17, 2020
Submission deadline for papers	April 24, 2020
Notification of acceptance	June 5, 2020
Final version due	July 3, 2020

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