

Call for Papers

The 33rd International Workshop on Logic & Synthesis (IWLS)

June 6-7, 2024, ETH Zurich, Switzerland

www.iwls.org

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The International Workshop on Logic and Synthesis is the premier forum for research in synthesis, optimization, and verification of integrated circuits and systems. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop encourages the early dissemination of ideas and results. The workshop accepts complete papers highlighting important new problems in the early stages of development, without providing complete solutions. The emphasis is on novelty and intellectual rigor.

Topics of interest include but are not limited to: hardware synthesis and optimization; software synthesis; hardware/software co-synthesis; power and timing analysis; testing, validation, and verification; synthesis for reconfigurable architectures; hardware compilation for domain-specific languages; and design experiences. Submissions on modeling, analysis, and synthesis for emerging technologies and platforms are particularly encouraged.

The workshop format includes paper presentations, invited talks, social lunch and dinner gatherings, and recreational activities.

Call for regular papers: Only complete papers with original and previously unpublished material are permitted. Submissions must be no longer than 8 pages (reference excluded), double column, 10-point font (we recommend using the [ACM template](#) or the [IEEE template](#), but not necessary). Accepted papers are distributed only to IWLS participants. Submissions are made electronically through [EasyChair](#). Please see the workshop website for instructions: www.iwls.org.

Double-blind policy: IWLS uses a double-blind reviewing system. Manuscripts must not identify authors or their affiliations; those that do will not be considered.

Paper abstract submission: ~~March 29, 2024~~ **April 5, 2024 (AoE)**
Submission deadline for papers: ~~April 5, 2024~~ April 12, 2024 (AoE)
Notification of acceptance: May 6, 2024
Final version due: May 31, 2024
Submission link: <https://easychair.org/conferences/?conf=iwls2024>

Keynotes

Can AI design and verify your design?

Ziyad Hanna, Cadence Design Systems, Israel

Symmetric is better: can we exploit regularities in logic synthesis?

Valentina Ciriani, University of Milano, Italy

Programming Contest

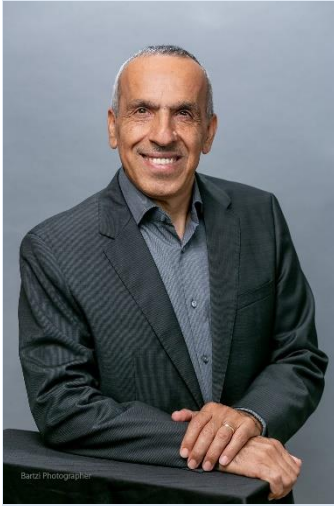
We have an exciting logic synthesis contest with prizes this year (1st place: \$800, 2nd place: \$400, 3rd place: \$300). See the next page for details.

Technical Program Committee

Luca Amaru, Synopsys
Anna Bernasconi, Università di Pisa
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Zhufei Chu, Ningbo University
Valentina Ciriani, Università degli Studi di Milano
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Winston Haaswijk, Cadence Design Systems
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Bruno Schmitt, Nvidia
Mathias Soeken, Microsoft
Eleonora Testa, Synopsys
Tiziano Villa, Università degli Studi di Verona
Robert Wille, TU Munich & SCCH GmbH
Xiaoqing Xu, X, the moonshot factory
Cunxi Yu, University of Maryland

Keynotes Details



Can AI design and verify your design?
Ziyad Hanna, Cadence Design Systems, Israel

Ziyad Hanna, Ph.D., is currently a corporate VP at Cadence Design Systems (CDNS), and the general manager of Cadence Israel, leading R&D centers in various countries, in the electronic design automation domain. Prior to joining Cadence Design Systems, Dr. Hanna was a Senior VP at Jasper Design Automation, which was acquired by Cadence in 2014. At Jasper, Dr. Hanna worked in the fast-emerging domain of formal verification technology and applications. Dr. Hanna was also an Intel Senior Principal Engineer and R&D Group Leader at Intel Haifa, where he was instrumental in the development of several generations of formal verification systems, which were used on almost all Intel microprocessor designs since early 1990s, and was twice the recipient of Intel's highest Achievement Award (IAA). He received both his BS and MS degrees in Computer Science at Tel Aviv University, and his PhD in Computer Science from the University of Oxford. Besides his leadership at Cadence, Prof. Hanna is currently serving as a visiting professor of Computer Science at Oxford. Dr. Hanna is a senior IEEE member, holds over 15 patents, and has published more than 80 papers and talks.



Symmetric is better: can we exploit regularities in logic synthesis?
Valentina Ciriani, University of Milano, Italy

Valentina Ciriani received the Laurea degree and the Ph.D. degree in Computer Science from the University of Pisa, Italy, in 1998 and 2003, respectively. In 2003 and 2004 she was with the Department Computer Science at University Pisa, Italy as a Ph.D. fellow. From 2005 to 2015 she was an assistant professor in Computer Science at the Department of Computer Science, University of Milano, Italy. She is currently an Associate Professor in Computer Science with the Department of Computer Science of the University of Milano (Italy). Her research interests include algorithms and data structures, as well as combinational logic synthesis for classical and emerging technologies. She has authored or coauthored more than 100 research papers, published in international journals, conference proceedings, and books chapters.

Programming Contest Details

In 2022 and 2023, IWLS Programming Contest focused on synthesizing the smallest possible correct circuits for a suite of Boolean functions representative of hardware designs, including random logic, arithmetic operators, and typical functionality of artificial neurons in machine learning. This is the motivation to have this year's competition closely resemble the last year's competition when it comes to the rules, and only change the set of benchmarks used. As indicated in the IWLS 2023 Programming Contest announcement, we expect the participants to submit two sets of solutions, containing and-inverter graphs (AIGs) and xor-and-inverter graphs (XAIGs) for the given test cases. The results will be evaluated using the same criteria as in 2023.

We encourage the participant to carefully study the announcement of the past two competitions-which you can find in the official call for submissions-for other helpful information, including verification of the solutions using ABC.

You can find the official call for submissions with more details [here](#).

To download the programming contest benchmarks, click [here](#).

Visit the [submission website](#) to submit your results.

The contest submission deadline is May 31, 2024.

This year's programming contest prizes:

1st place: \$800,-

2nd place: \$400,-

3rd place: \$300,-