Call for Papers

The 31st International Workshop on Logic & Synthesis (IWLS)

July 18 – 21, 2022
Virtual Conference

www.iwls.org

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Synopsys, USA

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The International Workshop on Logic and Synthesis is the premier forum for research in synthesis, optimization, and verification of integrated circuits and systems. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop encourages early dissemination of ideas and results. The workshop accepts complete papers highlighting important new problems in the early stages of development, without providing complete solutions. The emphasis is on novelty and intellectual rigor.

Topics of interest include, but are not limited to: hardware synthesis and optimization; software synthesis; hardware/software co-synthesis; power and timing analysis; testing, validation and verification; synthesis for reconfigurable architectures; hardware compilation for domain-specific languages; and design experiences. Submissions on modeling, analysis and synthesis for emerging technologies and platforms are particularly encouraged.

Call for regular papers: Only complete papers with original and previously unpublished material are permitted. Submissions must be no longer than 8 pages, double column, 10-point font. Accepted papers are distributed only to IWLS participants. The workshop format includes paper presentations, posters, invited talks and social coffee breaks. Submissions are made electronically through EasyChair. Please see the workshop website for instructions.

Important Dates

<table>
<thead>
<tr>
<th>Event</th>
<th>Date</th>
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<tr>
<td>Paper abstract submission</td>
<td>April 11, 2022</td>
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<tr>
<td>Submission deadline for papers</td>
<td>April 18, 2022 @ 11.59pm Anywhere on Earth</td>
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<td>Notification of acceptance</td>
<td>June 24, 2022</td>
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<td>Final version due</td>
<td>July 06, 2022</td>
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IWLS 2022 Programming Contest

The goal of this year’s contest is to synthesize small circuits for completely-specified multi-output Boolean functions represented using truth tables. Participants should find competitive solutions for different benchmarks using a variety of novel break-through methods (e.g., search and enumeration, new decomposition, etc.).

To participate, check out the contest description and download the benchmark. More details on the submission rules and deadlines will be available soon.

Technical Program Committee

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