Call for Papers

The 33rd International Workshop on Logic & Synthesis (IWLS)

June 6-7, 2024, ETH Zurich, Switzerland

www.iwls.org

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The International Workshop on Logic and Synthesis is the premier forum for research in synthesis, optimization, and verification of integrated circuits and systems. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop encourages the early dissemination of ideas and results. The workshop accepts complete papers highlighting important new problems in the early stages of development, without providing complete solutions. The emphasis is on novelty and intellectual rigor.

Topics of interest include but are not limited to: hardware synthesis and optimization; software synthesis; hardware/software co-synthesis; power and timing analysis; testing, validation, and verification; synthesis for reconfigurable architectures; hardware compilation for domain-specific languages; and design experiences. Submissions on modeling, analysis, and synthesis for emerging technologies and platforms are particularly encouraged.

The workshop format includes paper presentations, invited talks, social lunch and dinner gatherings, and recreational activities.

Call for regular papers: Only complete papers with original and previously unpublished material are permitted. Submissions must be no longer than 8 pages, double column, 10-point font. Accepted papers are distributed only to IWLS participants. Submissions are made electronically through EasyChair. Please see the workshop website for instructions: www.iwls.org.

Paper abstract submission: March 29, 2024
Submission deadline for papers: April 5, 2024
Notification of acceptance: May 6, 2024
Final version due: May 31, 2024
Submission link: https://easychair.org/conferences/?conf=iwls2024

IWLS 2024 Programming Contest

The goal of this year's contest is to synthesize the smallest possible circuits for a suite of Boolean functions representative of hardware designs, including random logic, arithmetic operators, and artificial neurons in machine learning. For more details, please check the contest description on the workshop website. The contest submission deadline is May 31, 2024.

Technical Program Committee (Tentative)

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