



Call for Papers

The 36th International Workshop on Logic & Synthesis (IWLS 2027)

May 17-19, 2027, Shanghai, China

<https://www.iwls.org>

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The International Workshop on Logic and Synthesis is the premier forum for research in synthesis, optimization, and verification of integrated circuits and systems. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop encourages the early dissemination of ideas and results. The workshop accepts complete papers highlighting important new problems in the early stages of development, without providing complete solutions. The emphasis is on novelty and intellectual rigor.

Topics of interest include but are not limited to: hardware synthesis and optimization; software synthesis; hardware/software co-synthesis; power and timing analysis; testing, validation, and verification; synthesis for reconfigurable architectures; hardware compilation for domain-specific languages; and design experiences. Submissions on modeling, analysis, and synthesis for emerging technologies and platforms are particularly encouraged.

The workshop format includes paper presentations, invited talks, social lunch and dinner gatherings, and recreational activities.

Call for regular papers: Only complete papers with original and previously unpublished material are permitted. Submissions must be no longer than 8 pages (references excluded), double column, 10-point font (we recommend using the [ACM template](#) or the [IEEE template](#), but not necessarily). Accepted papers are distributed only to IWLS participants.

Double-blind policy: IWLS uses a double-blind reviewing system. Manuscripts must not identify authors or their affiliations; those that do will not be considered.

If you have questions about how to meet these guidelines, please contact the [program chairs](#) before the submission deadline.

The submission page will be announced here.

Paper abstract submission: February 8, 2027 (AoE) (same for special sessions)

Full paper submission: February 15, 2027 (AoE)

Notification of acceptance: March 21, 2027 (AoE)

Final version due: May 8, 2027 (AoE)

Special Sessions

Quantum Logic Synthesis: synthesis, optimization, and verification of quantum circuits and systems, including gate mapping and compilation for NISQ and fault-tolerant devices.

Computing-in-Memory Synthesis: synthesis and compilation for in-memory computing platforms, including mapping logic and neural-network workloads onto memristor/ReRAM/SRAM-based arrays.

Special session papers: Special session papers: same format and deadlines as regular papers.

Technical Program Committee

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